Features

- Integrated 6 fast recovery power MOSFETs (500V/5A)
- Integrated high voltage gate drive circuit
- Compatible with 3.3V&5V input signal,effective at high level
- Integrated temperature output
- Built-in quick recovery bootstrap diode
- Insulation class 1500Vrms / min
- Integrated bootstrap functionality
- High reliability and thermal stability,good parameter consistency

DIP-23

SOP-23

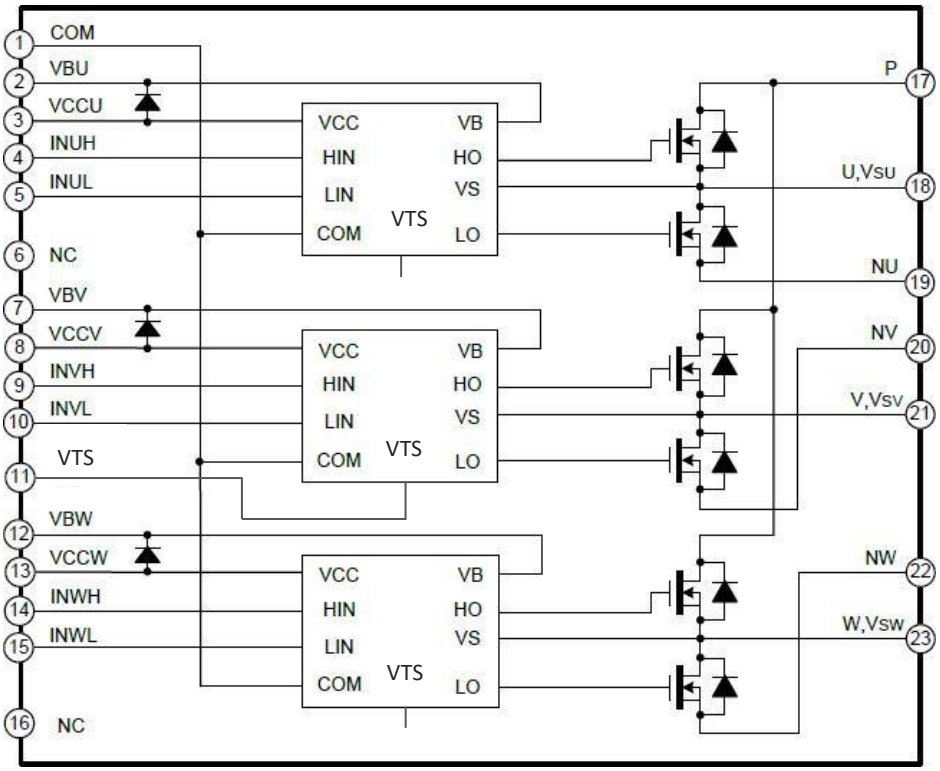
Applications

- Frequency converter
- Air Conditioning compressor
- Air cleaner
- Dish washer
- Cooker hood

Ordering Information

Product Name	Marking	Package Type
SYIM05M50BTD	SYIM05M50BTD	SOP-23H
SYIM05M50BTA	SYIM05M50BTA	DIP-23H

Internal Electrical Schematic



Absolute Maximum Ratings: T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
DC link supply voltage of P- N	V_{PN}	500	V
Single MOSFET output current ,T_C=25°C	I_{D25}	5	A
Single MOSFET peak output current T_C=25 C, pulse width < 100 μs	I_{DP}	9	A
Power dissipation per MOSFET,T_C=25°C	P_D	-	W
Module supply voltage	V_{CC}	25	V
High side floating supply voltage (V_B reference to V_S)	V_{BS}	20	V
Input voltage	V_{IN}	-0.3~VCC+0.3	V
Operating junction temperature	T_J	-55 to 150	°C
Operating case temperature,T_J≤ 150°C	T_C	-40 to 125	°C
Storage temperature range	T_{STG}	-40 to 125	°C
Single MOSFET thermal resistance, junction- case	$R_{\theta JC}$	-	°C/W
Isolation test voltage (1min, RMS, f = 60Hz)	V_{ISO}	1500	Vrms

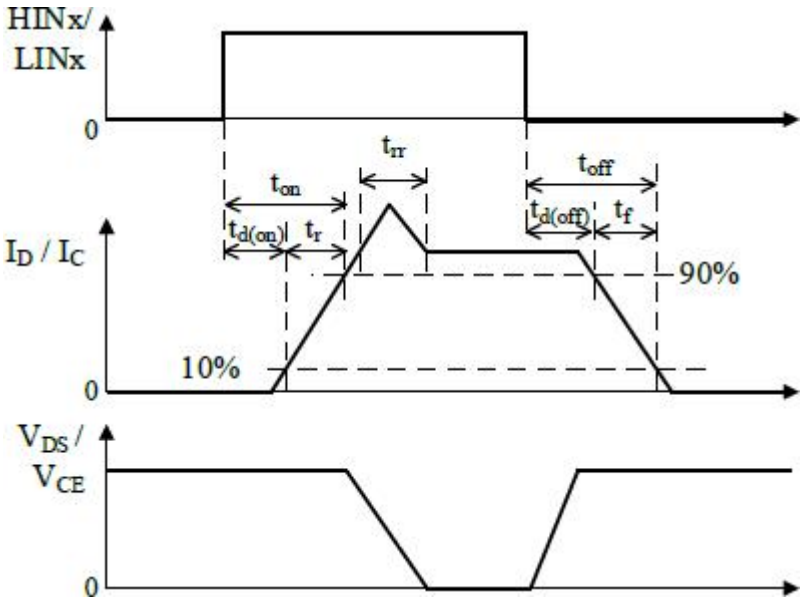
Recommended Operation Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	-	300	400	V
Low side supply voltage	V_{CC}	10	15	20	V
High side floating supply voltage	V_{BS}	V_S+10	V_S+15	V_S+20	V
Logic "1" input voltage (LIN, HIN)	VIN(ON)	2.5	-	-	V
Logic "0" input voltage (LIN, HIN)	VIN(OFF)	-	-	0.8	V
External deadtime between HIN and LIN	T_{dead}	-	450	-	ns

Electrical Characteristics（unless otherwise noted，T_J=25℃，V_{CC}=V_{BS}=15V）

Inverter section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Drain-Source blocking voltage	B_{VDSS}	V_{IN}=0V，I_D=250uA	500	-	-	V
Drain-Source leakage current	I_{DSS}	V_{DS}=600V,V_{GS}=0V	-	-	1	uA
Drain-Source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	-	1.3	-	Ω
Diode forward voltage	V_{SD}	V_{SG}=0V, I_s=3.5A	-	0.9	-	V
Switching time	t_{ON}	V_{PN}=300V,V_{CC}=V_{BS}=15V I_D=5A, V_{IN}=0V~5V, Inductive load	-	920	-	ns
	t_{OFF}		-	661	-	ns
	t_{rr}		-	89	-	ns
	E_{ON}		-	132	-	uJ
	E_{OFF}		-	2.3	-	uJ



Switching Time Definition

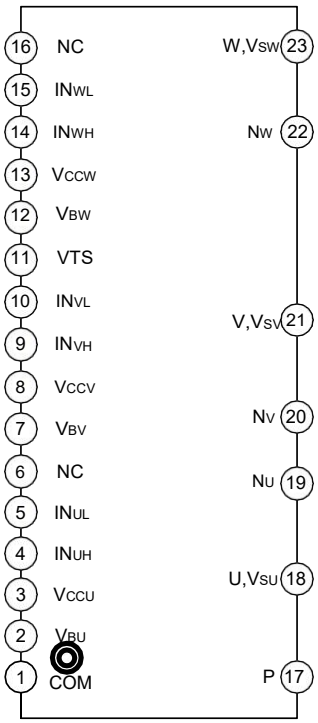
Control section

Parameter	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Quiescent V_{CC} supply current	I_{QCC}	VBIAS (V_{CC}, V_{BS}) =15V T_A =25°C		-	160	-	uA
Quiescent V_{BS} supply current	I_{QBS}			-	70	-	uA
Temperature Output	VTS	V phase HVIC temperature @25°C		600	790	980	mV
		V phase HVIC temperature @100°C		-	2.15	-	V
Low side undervoltage protection	UV_{CCR}	Reset level		8	8.9	9.8	V
High side undervoltage protection	UV_{BSR}	Reset level		8	8.9	9.8	V
Logic "1" input voltage (LIN, HIN)	V_{IH}	Logic high level	Between input and COM	2.5	-	-	V
Logic "0" input voltage (LIN, HIN)	V_{IL}	Logic Low level		-	-	0.8	V
Input bias current for LIN, HIN	I_{IH}	V_{IN}=5V	Between input and COM	-	6	15	uA
	I_{IL}	V_{IN}=0V		-	-	1	

Bootstrap diode section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Forward voltage	V_F	I_F=10mA@ T_j =25°C	-	2.3	-	V
Bootstrap Diode Resistance	R_{BS}	I_F=10mA@ T_j =25°C	-	289	-	Ω

Pin Assignment



Pin Description

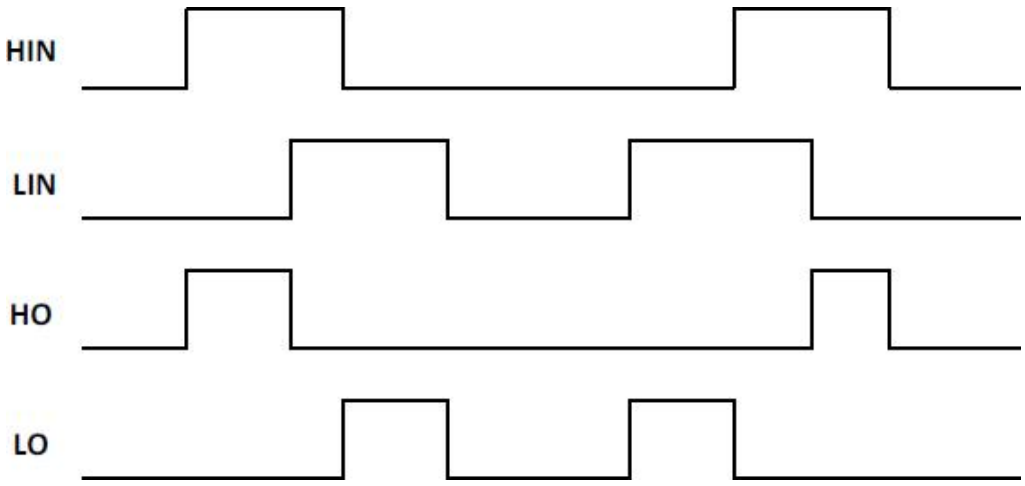
Pin Number	Pin Name	I/O	Pin Description
1	COM	I/O	Module common ground
2	V_{BU}	I/O	U-phase high side floating IC supply voltage
3	V_{CCU}	I/O	U-phase low side driver supply voltage
4	IN_{UH}	I	U-phase high side gate driver input
5	IN_{UL}	I	U-phase low side gate driver input
6	NC	I/O	No Connection
7	V_{BV}	I/O	V-phase high side floating IC supply voltage
8	V_{CCV}	I/O	V-phase low side driver supply voltage
9	IN_{VH}	I	V-phase high side gate driver input
10	IN_{VL}	I	V-phase low side gate driver input
11	VTS	O	Temperature sensing output signal
12	V_{BW}	I/O	W-phase high side floating IC supply voltage
13	V_{CCW}	I/O	W-phase low side driver supply voltage
14	IN_{WH}	I	W-phase high side gate driver input
15	IN_{WL}	I	W-phase low side gate driver input
16	NC	I/O	No Connection
17	P	I/O	Positive bus input voltage
18	U,V_{SU}	O	Motor U-phase output and U-phase high side drive bias voltage ground
19	N_U	I/O	U-phase low side source

Pin Number	Pin Name	I/O	Pin Description
20	N_V	I/O	V-phase low side source
21	V,V_{SV}	O	Motor V-phase output and V-phase high side drive bias voltage ground
22	N_W	I/O	W-phase low side source
23	W,V_{SW}	O	Motor W-phase output and W-phase high side drive bias voltage ground

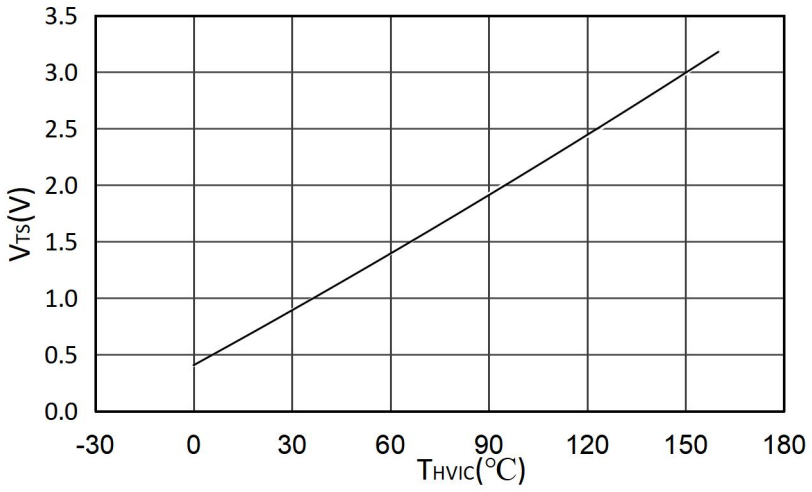
Function description

Input-output table

IN_H	IN_L	O_{UTPUT}	Remark
0	0	Z	The high and low sides of the bridge arm are closed
0	1	0	The low side of the bridge arm is opened
1	0	VDC	The high side of the bridge arm is opened
1	1	Forbid	Bridge arm punch through
Open	Open	Z	The high and low sides of the bridge arm are closed

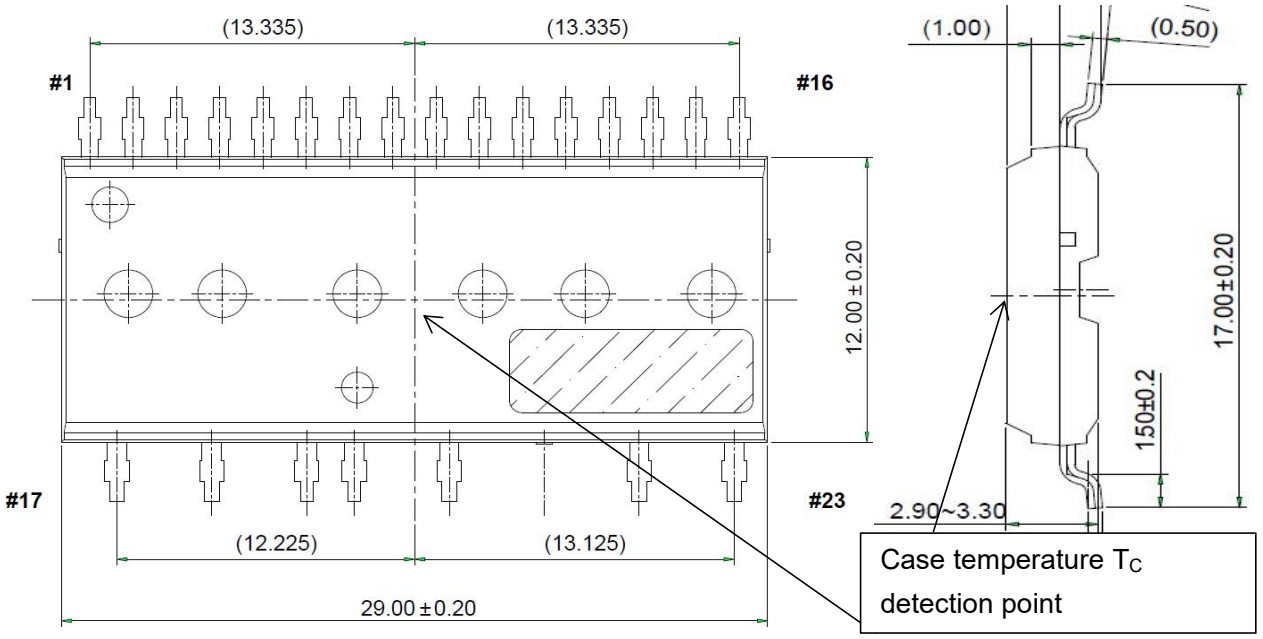


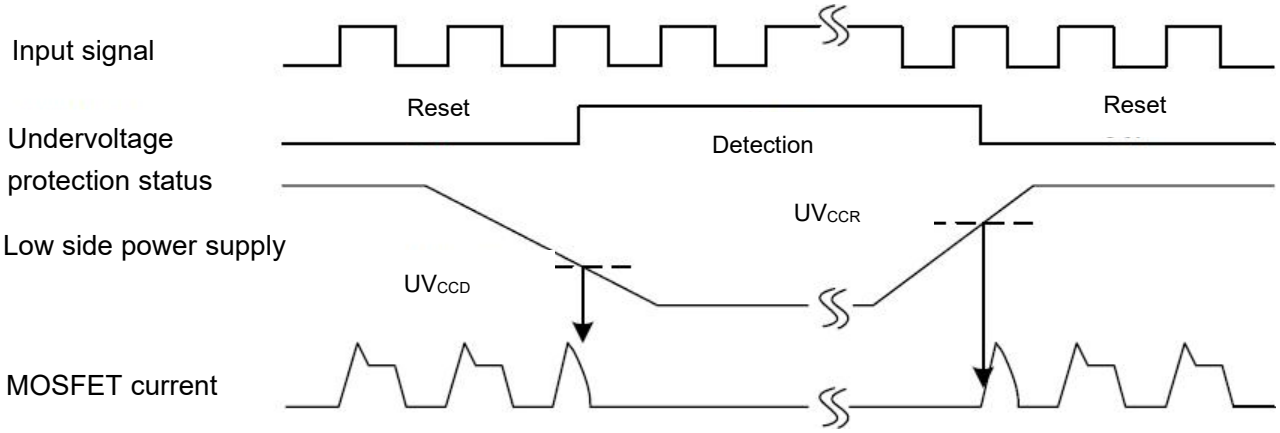
Control sequence diagram



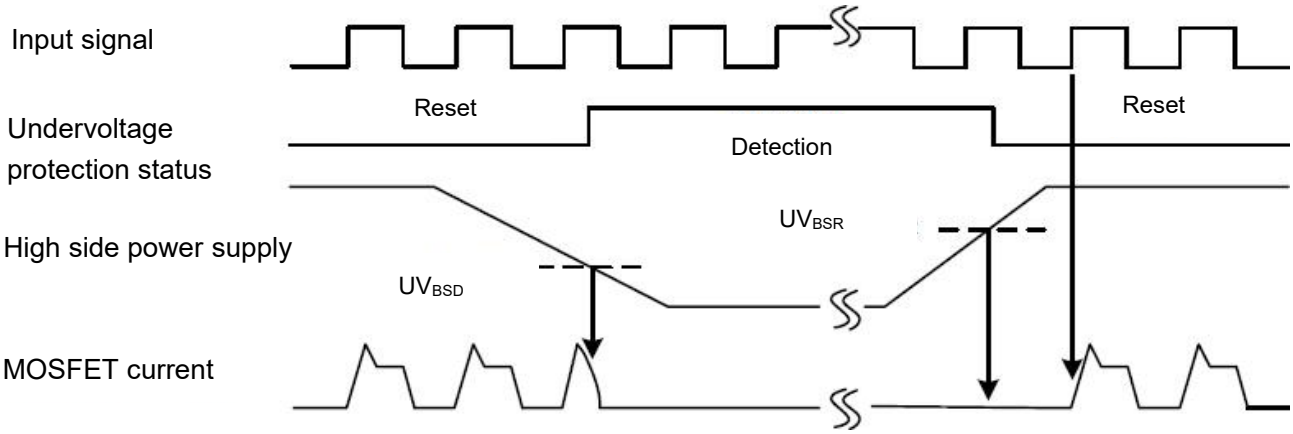
Temperature Profile of V_{TS}(Typical)

Case temperature T_C detection



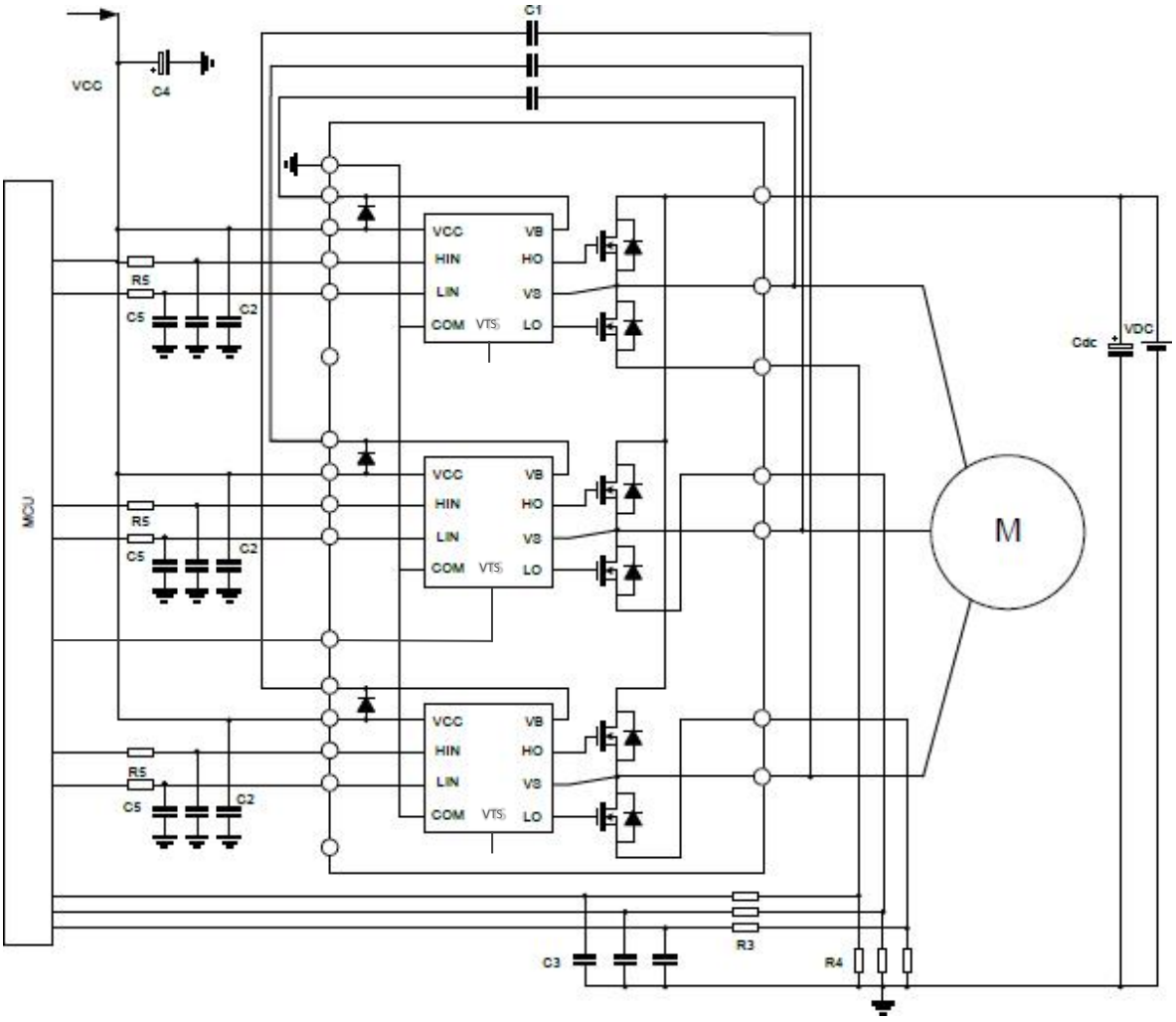


Undervoltage protection(Low side)



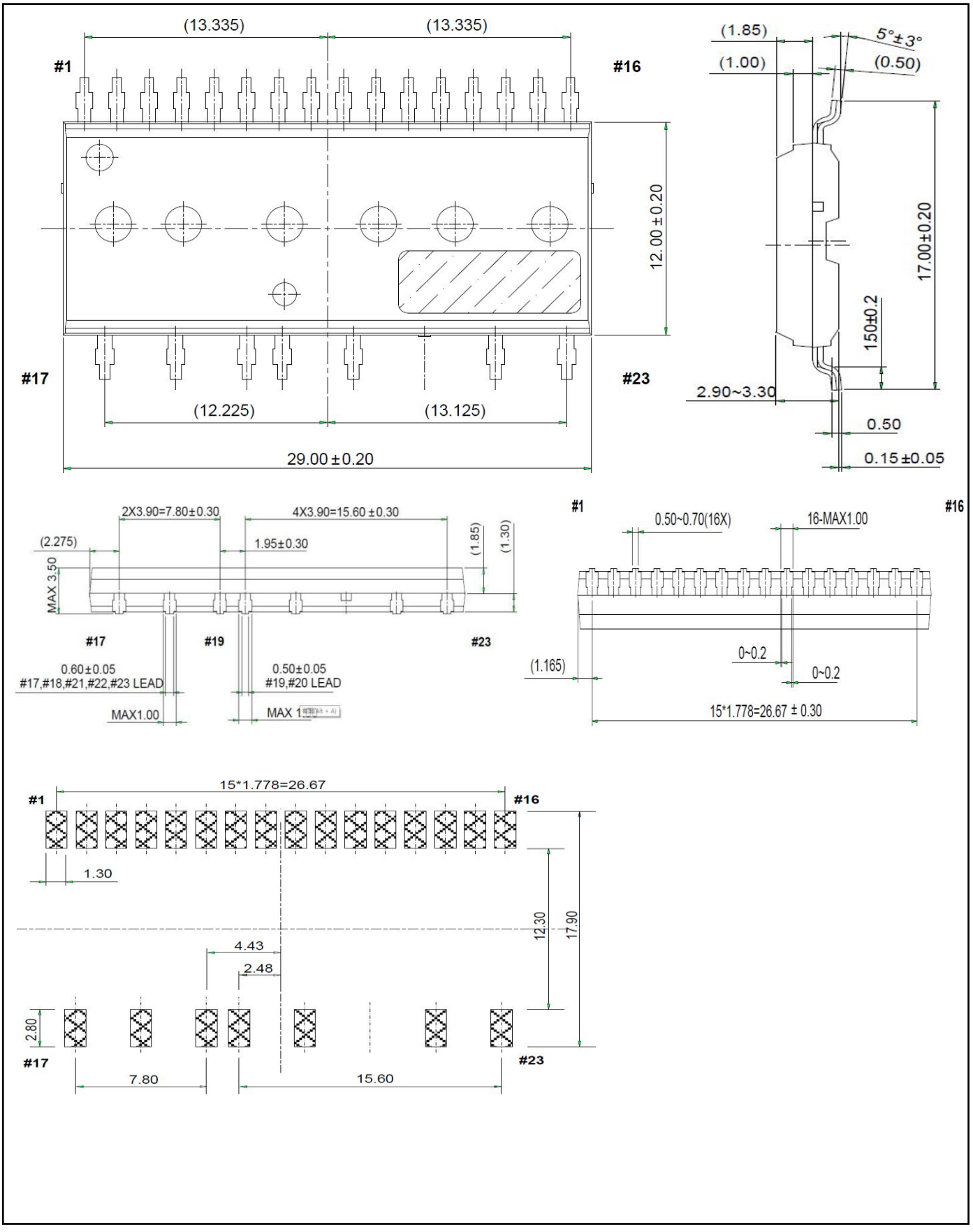
Undervoltage protection(High side)

Typical Application Schematic:



Remark:
(1)The wiring of each input pin shall be as short as possible, otherwise it may cause mis operation； in addition, RC filter can be used to reduce input signal noise.
(2)All external capacitors should be located close to IPM.
(3)In order to prevent surge damage, in addition to filter capacitance between PN, it is recommended to add a high-frequency non inductive smoothing capacitance, and the connection of capacitance should be as short as possible.
(4)The filter capacitance at the input of VCC power supply is recommended to be at least 7 times of bootstrap capacitance C1.
(5)The bootstrap capacitor C1 is suggested to adopt a capacitor with high frequency characteristics to absorb high frequency ripple current, and its capacitance value is suggested to be greater than 2.2uf.
(6)The connection between current limiting resistor R4 and IPM shall be as short as possible to prevent the large surge voltage generated by the connection inductance from damaging IPM.

Package Outline SOP-23H



Package Outline DIP-23H